In the Claims:

Claims 1-17 (CANCELLED)

18. (PREVIOUSLY PRESENTED) A method for reducing transfer latencies in fencepost buffering associated with a network controller and a host entity with shared memory, the method comprising the steps of:

providing a cache between the network controller and the host entity;

fetching a first and second descriptor address location from the shared memory wherein the first descriptor address location is a location of an active descriptor and the second descriptor address location is a location of a reserve descriptor;

copying the active descriptor to the cache; and

issuing a command to a direct memory access unit (DMA) of the network controller for transfer of the active descriptor back to the shared memory.

19. (PREVIOUSLY PRESENTED) The method according to claim 18, and further comprising the step of holding the active descriptor as a current descriptor within a top cache.

20. (PREVIOUSLY PRESENTED) The method according to claim 19, and further comprising the step of copying a reserve descriptor from a bottom cache into the top cache when the current descriptor in the top cache is consumed.

21. (PREVIOUSLY PRESENTED) The method according to claim 20, and further comprising the step of fetching the next descriptor in an external ring of descriptors when the reserve descriptor is copied into the top cache.

22. (PREVIOUSLY PRESENTED) The method of claim 20, and further comprising the step of copying the second descriptor address location into the first descriptor address location after the active descriptor is copied to the top cache.

23. (PREVIOUSLY PRESENTED) The method of claim 18, further comprising the steps of:

fetching a next descriptor address location from the shared memory; and

placing the next descriptor address location in the second descriptor address location.

24. (PREVIOUSLY PRESENTED) The method of claim 18, further comprising the step of updating the ownership of terminal descriptors associated with a frame, the terminal descriptors comprising an End of Frame (EOF) descriptor and a Start of Packet (SOP) descriptor.

25. (PREVIOUSLY PRESENTED) The method of claim 24, wherein the step of updating the ownership of the terminal descriptors further comprises the step of writing the EOF descriptor to the shared memory before writing the SOP descriptor to the shared memory.

26. (PREVIOUSLY PRESENTED) The method of claim 25, further comprising the step of setting an ownership bit in the EOF descriptor when the EOF descriptor is the active descriptor.

27. (PREVIOUSLY PRESENTED) The method of claim 26, further comprising the step of:

re-editing the active descriptor to build an image of the SOP descriptor;

copying the SOP descriptor to the cache; and

issuing a command to the DMA requesting transfer of the SOP descriptor to shared memory.

28. (PREVIOUSLY PRESENTED) A method for reducing transfer latencies in fencepost buffering having chained descriptors including an End of Frame (EOF) descriptor and a Start of Packet (SOP) descriptor, defining terminal descriptors, associated with a frame, the method comprising the steps of:

providing a cache between a host and a network controller having shared memory;

fetching a first and second descriptor address location from shared memory wherein the first descriptor address location is a location of an active descriptor and the second descriptor address location is a location of a reserve descriptor; and

updating ownership of terminal descriptors by writing the EOF descriptor of the frame to the shared memory before writing the SOP descriptor of the frame to the shared memory; and

issuing a command to a direct memory access unit (DMA) for transfer of the active descriptor back to the shared memory.

29. (PREVIOUSLY PRESENTED) The method according to claim 28, and further comprising the step of holding the active descriptor as a current descriptor within a top cache.

30. (PREVIOUSLY PRESENTED) The method according to claim 29, and further comprising the step of copying a reserve descriptor from a bottom cache into the top cache when the current descriptor in the top cache is consumed.

31. (PREVIOUSLY PRESENTED) The method according to claim 30, and further comprising the step of fetching the next descriptor in external ring of descriptors when the reserve descriptor is copied into the top cache.

32. (PREVIOUSLY PRESENTED) The method of claim 30, wherein the step of updating the terminal descriptors further comprises the steps of:

re-editing the active descriptor to build an image of the SOP descriptor; and

copying the SOP descriptor to the bottom cache.

33. (PREVIOUSLY PRESENTED) The method of claim 28, further comprising the step of copying the second descriptor address location into the first descriptor address location after the active descriptor is copied to the cache.

34. (PREVIOUSLY PRESENTED) The method of claim 33, further comprising the steps of:

fetching a next descriptor address location from the shared memory; and

placing the next descriptor address location in the second descriptor address location.

35. (PREVIOUSLY PRESENTED) A system for reducing transfer latencies in fencepost buffering having chained descriptors including an End of Frame (EOF) descriptor and a Start of Packet (SOP) descriptor, defining terminal descriptors, associated with a frame, the system comprising:

a network controller including a direct memory access unit (DMA);

a host entity with shared memory;

a cache between said network controller and said host entity;

means for fetching a first and second descriptor address location from shared memory wherein the first descriptor address location is a location of an active descriptor and the second descriptor address location is a location of a reserve descriptor;

means for updating the ownership of terminal descriptors by writing the EOF descriptor of the frame to shared memory before writing the SOP descriptor of the frame to shared memory; and

means for issuing a command to DMA for transfer of the active descriptor back to the shared memory.

36. (PREVIOUSLY PRESENTED) The system according to claim 35, wherein said cache comprises a top cache the holds the active descriptor as a current descriptor.

37. (PREVIOUSLY PRESENTED) The system according to claim 36, wherein said cache comprises a bottom cache for holding a reserve descriptor that is copied into the top cache when the current descriptor in the top cache is consumed.

38. (PREVIOUSLY PRESENTED) The system according to claim 37, and further comprising an external ring of descriptors from which a descriptor is fetched when the reserve descriptor in the bottom cache is copied into the top cache.

39. (PREVIOUSLY PRESENTED) The system of claim 37, wherein the means for updating the terminal descriptors further comprises:

means for reediting the active descriptor to build an image of the SOP descriptor; and

means for copying the SOP descriptor to the bottom cache.

40. (PREVIOUSLY PRESENTED) The system of claim 35, further comprising means for copying the second descriptor address location into the first descriptor address location after the active descriptor is copied to the top cache.

41. (PREVIOUSLY PRESENTED) The system of claim 40, further comprising:

means for fetching a next descriptor address location from the shared memory; and

means for placing the next descriptor address location in the second address location.

42. (PREVIOUSLY PRESENTED) A system for reducing transfer latencies in fencepost buffering, associated with a network controller and a host entity with shared memory, and having chained descriptors including an End of Frame (EOF) descriptor and a Start of Packet (SOP) descriptor, defining terminal descriptors, associated with a frame, the system comprising:

a cache between the network controller and the host entity; and

a cache controller to fetch a first and second descriptor address location from shared memory, the first descriptor address location being a location of an active descriptor and the second descriptor address location being a location of a reserve descriptor, to update the ownership of terminal descriptors by writing the EOF descriptor of the frame to shared memory before writing the SOP descriptor of the frame to shared memory, and to issue a command to a direct memory access unit (DMA) of the network controller for transfer of the active descriptor back to the shared memory.

43. (PREVIOUSLY PRESENTED) The system according to claim 42, wherein said cache comprises a top cache the holds the active descriptor as a current descriptor.

44. (PREVIOUSLY PRESENTED) The system according to claim 43, wherein said cache comprises a bottom cache for holding a reserve descriptor that is copied into the top cache when the current descriptor in the top cache is consumed.

45. (PREVIOUSLY PRESENTED) The system according to claim 44, and further comprising an external ring of descriptors from which a descriptor is fetched when the reserve descriptor in the bottom cache is copied into the top cache.

46. (PREVIOUSLY PRESENTED) The system of claim 44, wherein the cache controller re-edits the active descriptor to build an image of the SOP descriptor, and copies the SOP descriptor to the bottom cache.

47. (PREVIOUSLY PRESENTED) The system of claim 44, wherein the cache controller copies the second descriptor address location into the first descriptor address location after the active descriptor is copied to the top cache.